

FIG.1

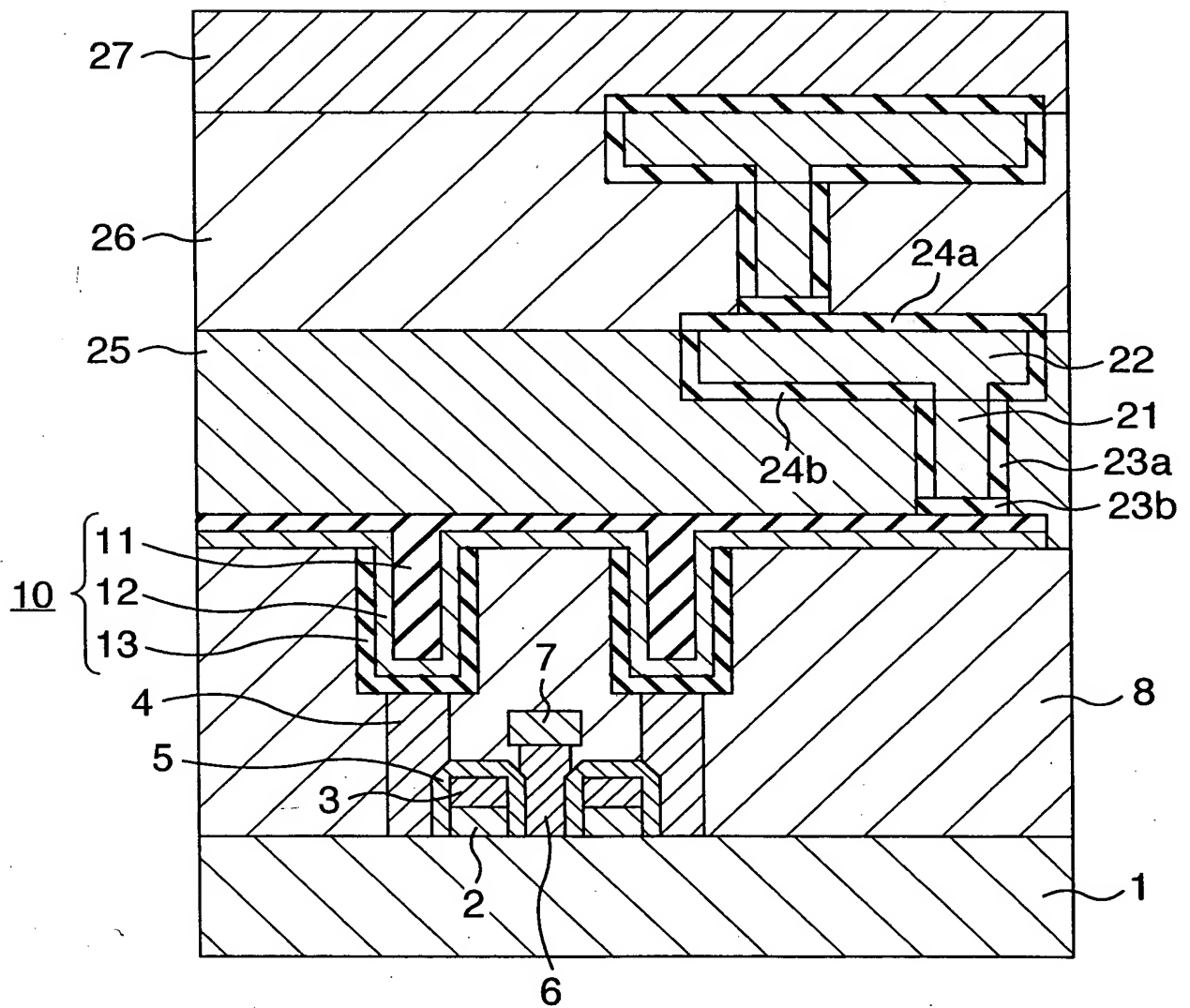


FIG.2

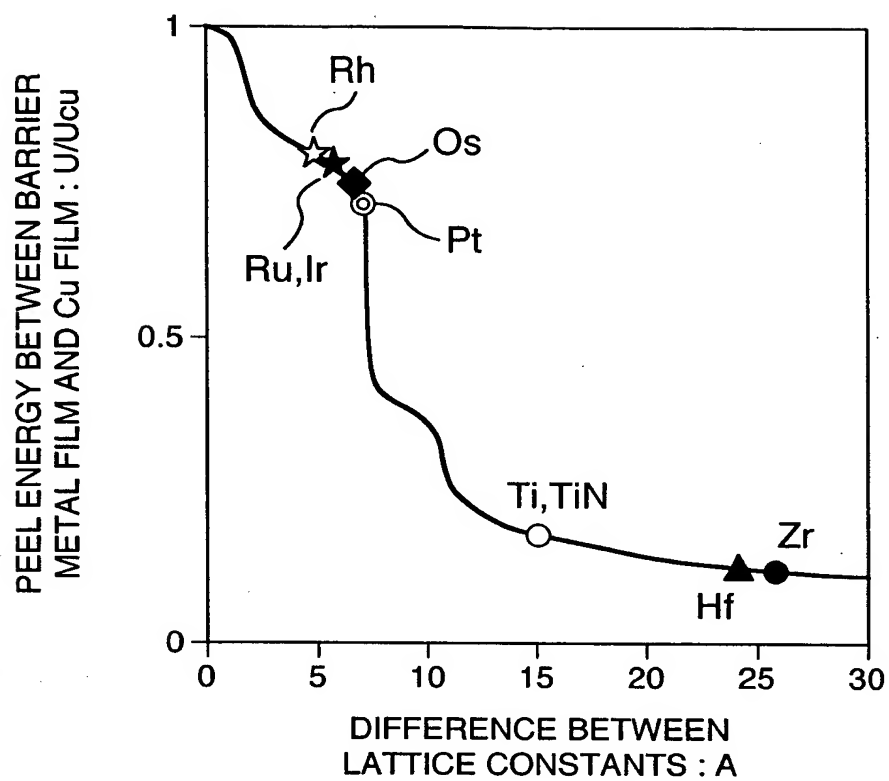


FIG.3

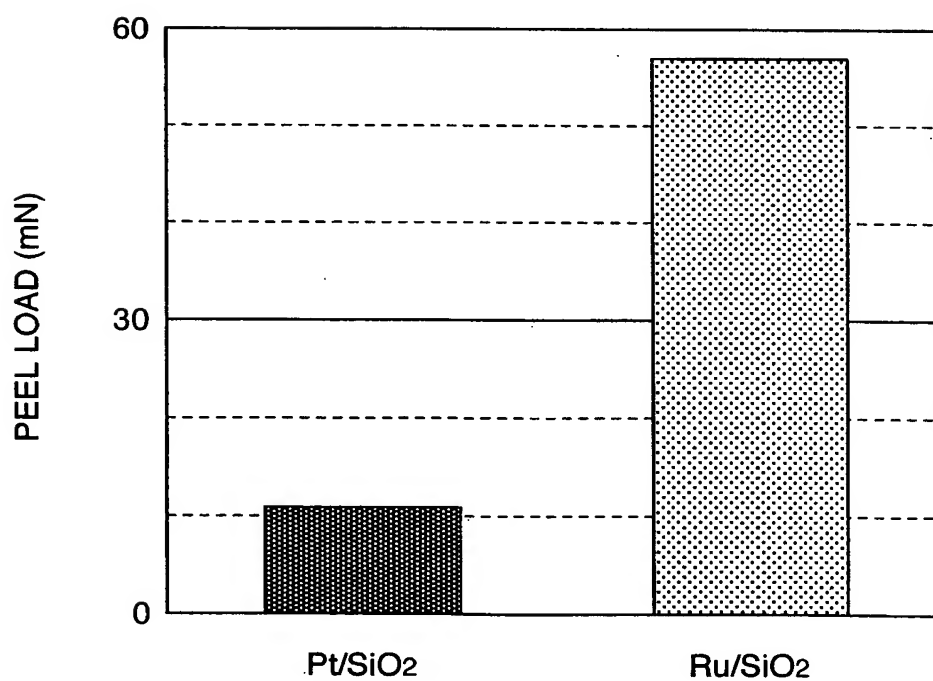


FIG.4

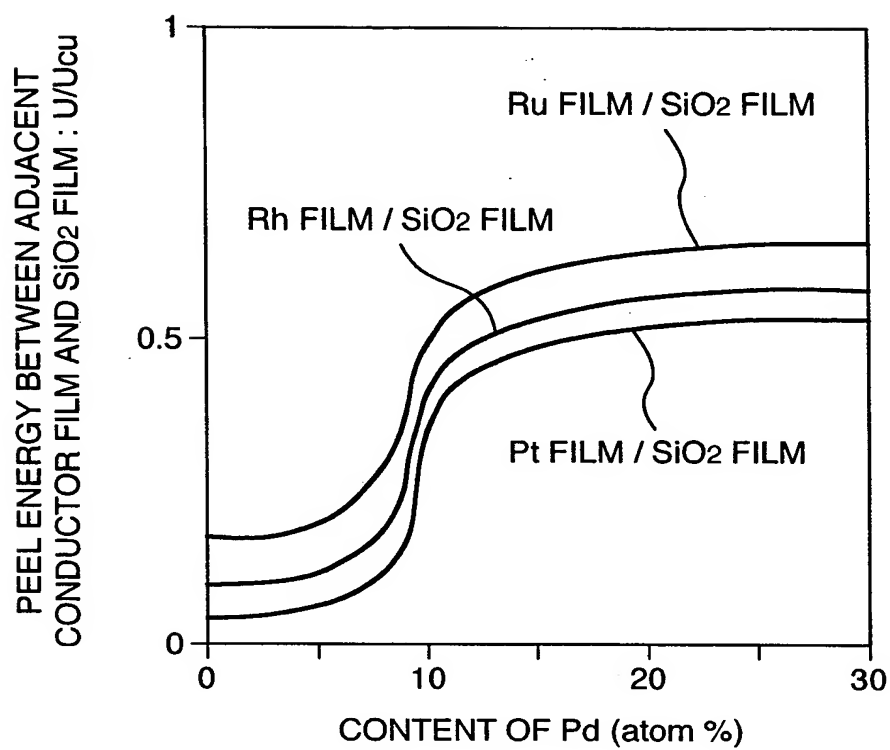


FIG.5

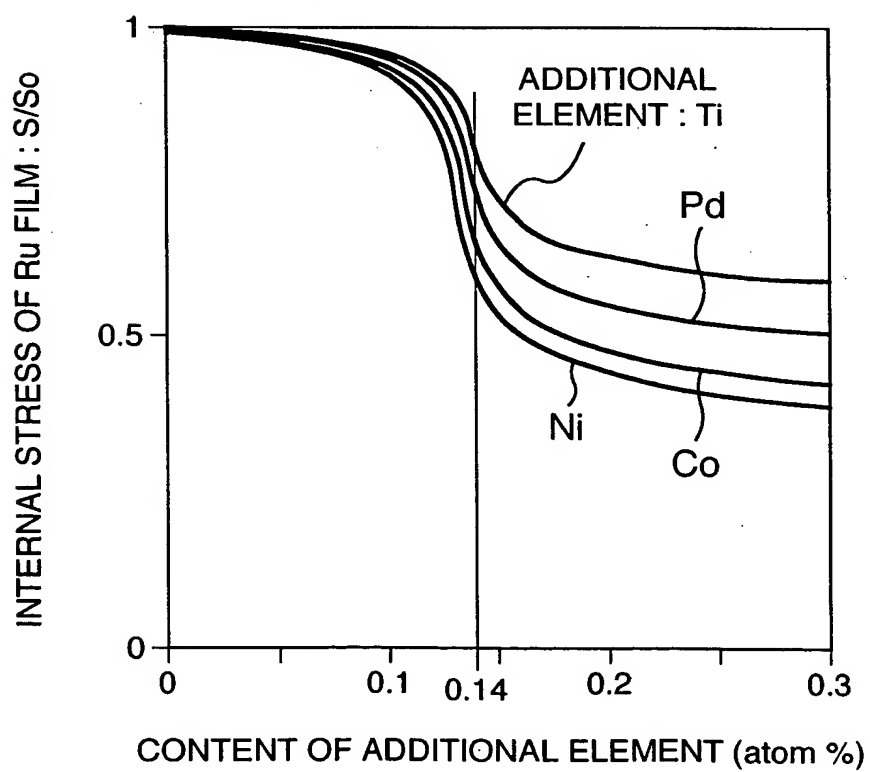
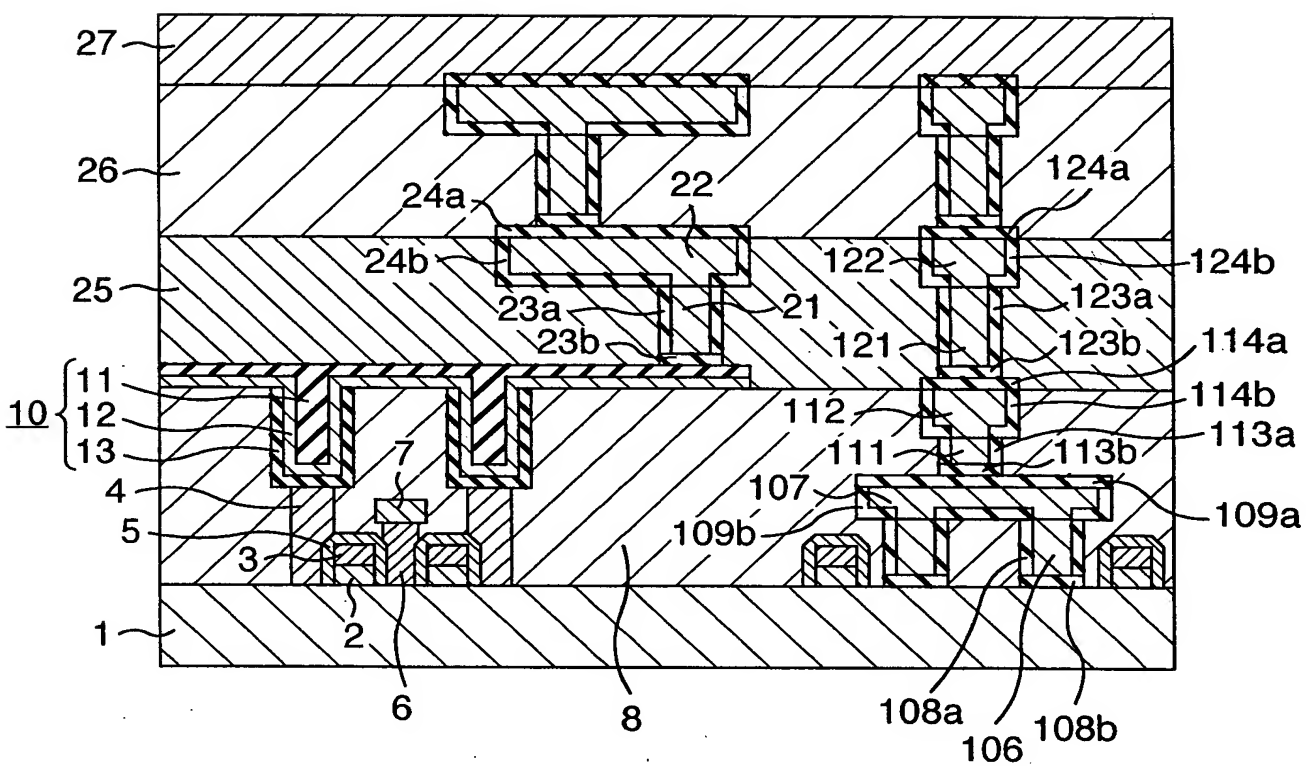


FIG.6



[illegible][illegible]

This cross-sectional view shows a semiconductor device with a substrate 1. A trench array 4 is formed in the substrate, with a bottom layer 5 and side walls 12, 13. A gate structure 7 is formed in the trench, consisting of a gate dielectric 3 and a gate electrode 2. A gate insulating layer 6 is formed on the top surface of the substrate. A gate electrode 8 is formed on the top surface of the gate insulating layer. A gate dielectric 107 is formed on the top surface of the gate electrode 8. A gate electrode 109b is formed on the top surface of the gate dielectric 107. A gate dielectric 109a is formed on the top surface of the gate electrode 109b. A gate electrode 111 is formed on the top surface of the gate dielectric 109a. A gate dielectric 112 is formed on the top surface of the gate electrode 111. A gate electrode 113b is formed on the top surface of the gate dielectric 112. A gate electrode 114b is formed on the top surface of the gate dielectric 113b. A gate electrode 108a is formed on the top surface of the gate dielectric 109a. A gate electrode 108b is formed on the top surface of the gate dielectric 109b.